In the Claims

Claims 1-20 are canceled.

21. [Original] A semiconductor processing method comprising forming two series of field effect transistors over a substrate, one series being isolated from adjacent devices by shallow trench isolation, the other series having active area widths greater than one micron, the one series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series.

22. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

23. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

24. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

25. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

26. [Previously Presented] A semiconductor processing method comprising forming two series of field effect transistors over a substrate, at least one series being isolated from adjacent devices by shallow trench isolation, and further comprising achieving different threshold voltages between field effect transistors in different series by varying the active area widths of the field effect transistors in the series providing a first series of transistors having active area widths less than active area widths of a second series of transistors and wherein the threshold voltages of the transistors of the first series are less than the threshold voltages of the transistors of the second series, at least one series having active area widths less than one micron.

27. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

28. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

29. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

30. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

Claims 31-60 are canceled.

61. [Previously Presented] The semiconductor processing method of claim 21, wherein the transistors of the two series comprise transistors having a single geometry type.

62. [Previously Presented] The semiconductor processing method of claim 61, wherein the transistors of the single geometry type comprise planar transistors.

63. [Previously Presented] The semiconductor processing method of claim 21, further comprising performing a common channel implant into active areas of the transistors of the two series at the same moment in time.

64. [Previously Presented] The semiconductor processing method of claim 21, further comprising performing a common channel implant into active areas of both of the series of the transistors at the same moment in time to define the different threshold voltages of the transistors of the two series.

65. [Previously Presented] The semiconductor processing method of claim 64, wherein the common channel implant is the only channel implant which defines the different threshold voltages of the transistors of the two series.

66. [Previously Presented] The semiconductor processing method of claim 21, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time.

67. [Previously Presented] The semiconductor processing method of claim 21, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time to simultaneously define the different threshold voltages of the transistors of the two series.

68. [Previously Presented] The semiconductor processing method of claim 67, wherein the implanting of the impurity is the only implant which defines the different threshold voltages of the transistors of the two series.

69. [Previously Presented] The semiconductor processing method of claim 22, wherein the common channel implant comprises implanting a single type of impurity.

70. [Currently Amended] The semiconductor processing method of claim 22, wherein the common channel implant comprises implanting a single type of impurity to define the ~~different voltage thresholds~~ threshold voltages of the transistors of the two series.

71. [Previously Presented] The semiconductor processing method of claim 26, wherein the transistors of the two series comprise transistors having a single geometry type.

72. [Previously Presented] The semiconductor processing method of claim 71, wherein the transistors of the single geometry type comprise planar transistors.

73. [Previously Presented] The semiconductor processing method of claim 26, further comprising performing a common channel implant into active areas of the transistors of the two series at the same moment in time.

74. [Previously Presented] The semiconductor processing method of claim 26, further comprising performing a common channel implant into active areas of both of the series of the transistors at the same moment in time to define the different threshold voltages of the transistors of the two series.

75. [Previously Presented] The semiconductor processing method of claim 74, wherein the common channel implant is the only channel implant which defines the different threshold voltages of the transistors of the two series.

76. [Previously Presented] The semiconductor processing method of claim 26, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time.

77. [Previously Presented] The semiconductor processing method of claim 26, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time to simultaneously define the different threshold voltages of the transistors of the two series.

78. [Previously Presented] The semiconductor processing method of claim 77, wherein the implanting of the impurity is the only implant which defines the different threshold voltages of the transistors of the two series.

79. [Previously Presented] The semiconductor processing method of claim 27, wherein the common channel implant comprises implanting a single type of impurity.

80. [Currently Amended] The semiconductor processing method of claim 27, wherein the common channel implant comprises implanting a single type of impurity to define the ~~different voltage thresholds~~ threshold voltages of the transistors of the two series.

81. [Previously Presented] The semiconductor processing method of claim 21, wherein the active area widths individually correspond to a dimension of an active area of a respective field effect transistor between plural shallow trench isolation regions immediately adjacent to opposing sides of the active area of the respective field effect transistor.

82. [Previously Presented] The semiconductor processing method of claim 26, wherein the active area widths individually correspond to a dimension of an active area of a respective field effect transistor between plural shallow trench isolation regions immediately adjacent to opposing sides of the active area of the respective field effect transistor.

83. [Previously Presented] The semiconductor processing method of claim 22, wherein the common channel implant comprises a channel implant into active areas of the field effect transistors of the two series.

84. [Previously Presented] The semiconductor processing method of claim 83, wherein an impurity of the common channel implant is implanted directly into the active areas of the field effect transistors of the two series.

85. [Previously Presented] The semiconductor processing method of claim 22, wherein the common channel implant comprises a channel implant into substantially entireties of the widths of active areas of the field effect transistors.

86. [Previously Presented] The semiconductor processing method of claim 85, wherein an impurity of the common channel implant is implanted directly into the active areas of the field effect transistors of the two series.

87. [Previously Presented] The semiconductor processing method of claim 86, wherein the impurity of the common channel implant is implanted into the active areas to form respective channels of the field effect transistors of the two series.

88. [Previously Presented] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a plurality of common channel implants which are individually implanted into active areas of the field effect transistors of the two series.

89. [Previously Presented] The semiconductor processing method of claim 88, wherein individual ones of the common channel implants are implanted directly into the active areas of the field effect transistors of the two series at the same moment in time.

90. [Previously Presented] The semiconductor processing method of claim 88, wherein the common channel implants individually comprise a channel implant into substantially entireties of the widths of the active areas of the field effect transistors.

91. [Previously Presented] The semiconductor processing method of claim 90, wherein the common channel implants are individually implanted directly into the active areas of the field effect transistors of the two series at the same respective moment in time.

92. [Previously Presented] The semiconductor processing method of claim 27, wherein the common channel implant comprises a channel implant into active areas of the field effect transistors of the two series.

93. [Previously Presented] The semiconductor processing method of claim 92, wherein an impurity of the common channel implant is implanted directly into the active areas of the field effect transistors of the two series at the same moment in time.

94. [Previously Presented] The semiconductor processing method of claim 93, wherein the impurity of the common channel implant is implanted into the active areas to form respective channels of the field effect transistors of the two series.

95. [Previously Presented] The semiconductor processing method of claim 27, wherein the common channel implant comprises a channel implant into substantially entireties of the widths of active areas of the field effect transistors.

96. [Previously Presented] The semiconductor processing method of claim 95, wherein an impurity of the common channel implant is implanted directly into the active areas of the field effect transistors of the two series at the same moment in time.

97. [Previously Presented] The semiconductor processing method of claim 26, wherein the achieving the different threshold voltages comprises performing a plurality of common channel implants which are individually implanted into active areas of the field effect transistors of the two series.

98. [Previously Presented] The semiconductor processing method of claim 97, wherein individual ones of the common channel implants are implanted directly into the active areas of the field effect transistors of the two series at the same moment in time.

99. [Previously Presented] The semiconductor processing method of claim 97, wherein the common channel implants individually comprise a channel implant into substantially entireties of the widths of the active areas of the field effect transistors.

100. [Previously Presented] The semiconductor processing method of claim 99, wherein the common channel implants are individually implanted directly into the active areas of the field effect transistors of the two series at the same respective moment in time.

101. [New] The semiconductor processing method of claim 22, wherein the common channel implant comprises a channel implant of an impurity into active areas of the field effect transistors prior to diffusion of the impurity.

102. [New] The semiconductor processing method of claim 22, wherein the common channel implant comprises a channel implant of an impurity into active areas of the field effect transistors without diffusion of the impurity.

103. [New] The semiconductor processing method of claim 27, wherein the common channel implant comprises a channel implant of an impurity into active areas of the field effect transistors prior to diffusion of the impurity.

104. [New] The semiconductor processing method of claim 27, wherein the common channel implant comprises a channel implant of an impurity into active areas of the field effect transistors without diffusion of the impurity.